

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO). <u> </u>	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/808,344		03/25/2004	Jun Koyama	0756-7274	5456	
31780	7590	08/01/2006		EXAMINER		
ERIC RO	BINSON		QUACH, TUAN N			
PMB 955 21010 SOU	JTHBANK	CST.		ART UNIT	PAPER NUMBER	
POTOMA	C FALLS,	VA 20165		2826		
				DATE MAILED: 08/01/2000	4	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicat	pplication No. Applicant(s)						
Office Action Summary			344	KOYAMA, JUN	KOYAMA, JUN				
			er	Art Unit					
		Tuan Qu	ach	2826					
Period fo	The MAILING DATE of this communicated reply	ation appears on th	e cover sheet with	the correspondence ac	idress				
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE MAINSIONS OF time may be available under the provisions of SIX (6) MONTHS from the mailing date of this communication period for reply is specified above, the maximum stature to reply within the set or extended period for reply with epity received by the Office later than three months after the patent term adjustment. See 37 CFR 1.704(b).	ILING DATE OF T 37 CFR 1.136(a). In no e lication. tory period will apply and v II, by statute, cause the ap	HIS COMMUNICA event, however, may a rep will expire SIX (6) MONTH oplication to become ABA	ATION. If you be timely filed HS from the mailing date of this of NDONED (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) filed	on 12 July 2006.							
•	This action is FINAL . 2b)⊠ This action is non-final.								
· —		pplication is in condition for allowance except for formal matters, prosecution as to the merits is							
٠,۵	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims	·	•						
4)⊠	Claim(s) 7-18 and 25-52 is/are pendin	a in the application	n.						
-	4a) Of the above claim(s) is/are withdrawn from consideration.								
	Claim(s) is/are allowed.								
•	Claim(s) <u>7-18 and 25-52</u> is/are rejected.								
7)	Claim(s) is/are objected to.								
8)□	Claim(s) are subject to restriction	on and/or election	requirement.						
Applicati	on Papers								
9)	The specification is objected to by the	Examiner.							
10)⊠ The drawing(s) filed on <u>25 March 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.									
.—	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority (ınder 35 U.S.C. § 119								
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:									
,	1.⊠ Certified copies of the priority documents have been received.								
	2. Certified copies of the priority documents have been received in Application No								
	3. Copies of the certified copies of the priority documents have been received in this National Stage								
	application from the International	al Bureau (PCT Ru	ule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.									
				14					
				Tuan Quach	l				
Attachmen				Primary Examir					
	e of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PT	0-048)	4) Interview Summary (PTO-413) Paper No(s)/Mail Date						
3) 🛛 Infor	ze of Draπsperson's Patent Drawing Review (P10 mation Disclosure Statement(s) (PTO-1449 or P er No(s)/Mail Date <u>7/12/06</u> .			otice of Informal Patent Application (PTO-152)					

DETAILED ACTION

Claims 7-18 and 25-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claims as amended and newly presented calls for a concentration of not greater than 5×10^{14} atoms/cm². Such open-ended range (at least to the lower range) appears to encompass between zero and (and including) 10^{14} atoms/cm². The specification however does not appear to provide support for such a range. See the specification page 5 lines 19-21 wherein it is disclosed that impurity may be doped at concentration of 5×10^{12} to 5×10^{14} atoms/cm². It does not appear that the specification sufficiently described or conveyed that the lower range outside the range disclosed in the instant specification (e.g., between zero and less than 5×10^{12} atoms/cm² can be employed, and that a range above 5×10^{14} atoms/cm² is not to be employed.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

For convenient referencing, et al. are omitted, e.g., Ogawa for Ogawa et al.

Claims 7-12, 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama taken with Ogawa and Chu.

Art Unit: 2826

Re claim 7, 33, Koyama 6,057,183 teaches a driver circuit including a shift register, a buffer circuit connected thereto including a source follower circuit comprising a polysilicon channel thin film transistor, an analog memory electrically connected to the buffer circuit. Koyama lacks primarily the recitation of the thin film transistor is a depletion mode transistor including the doped range. See Fig. 9, column 1 line 35 to column 2 line 23. Claims 10 and 36 recite the same except with the recitation of the product by process limitation of the polysilicon by crystallizing an morphous silicon not deemed patentable given substantially similar structure is disclosed and alternatively, such polysilicon by crystallizing amorphous silicon is notoriously conventional, in any event.

Ogawa 6,127,857 teaches the use of depletion-mode FETS to reduce power and enhance accuracy in the buffer circuit. See column 4 line 33 to column 5 line 35, column 6 lines 16-64. The provision of the polysilicon thin film transistor is also apparent, e.g., Fig. 13.

Chu 5,015,594 teaches channel implant to obtain the desired threshold voltage for depletion device, including for N channel and P channel using dosage of 1-10 x 10^{12} /cm². The recitation of conventional dopant such as boron and phosphorus and the selection of suitable dopants for respective NMOS or PMOS devices is also taught. See column 2 line 60 to column 4 line 28.

It would have been obvious to one skilled in the art in practicing the above invention in Koyama to have employed the thin-film transistors of depletion mode to obtain low power and or enhance accuracy in the buffer circuit as evidenced by Ogawa

Art Unit: 2826

and to include the channel implant including the suitable dosage and dopant employed as evidenced by Chu to obtain the desired threshold voltage. The selection of the desired range would have been obvious, as where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990); In re Geisler, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997). Similarly, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. Titanium Metals Corp. of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985)

"[A] prior art reference that discloses a range encompassing a somewhat narrower claimed range is sufficient to establish a prima facie case of obviousness." In re Peterson, 315 F.3d 1325, 1330, 65 USPQ2d 1379, 1382-83 (Fed. Cir. 2003).

Regarding claims 8, 11, 34, 37, the connection of the thin film transistor to an output terminal for electrical connection is well within the purview of one skilled in the art and as evidenced by Ogawa, column 6 line 21. Regarding claims 9, 12, 35, 38, the provision or selection of suitable substrates such as quartz or glass substrate is well within the purview of one skilled in the art, e.g., Koyama, column 1 lines 55-59, Ogawa et al., column 16 lines 1-2 and as such would have been obvious.

Claims 13-18, 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama taken with Ogawa, Chu, and Fujikura.

Application/Control Number: 10/808,344

Art Unit: 2826

Re claims 13, 16, 39, 42, these claims correspond to claims 7-12, 33-38 delineated above and would have been obvious for the same reason, the difference being the additional recitation of a bootstrap circuit, e.g., lines 3 in the claims. Koyama is applied as above and additionally does not recite the buffer circuit comprising a bootstrap circuit comprising the thin film transition in a depletion mode transistor. The product-by-process recitation of the polysilicon by crystallizing amorphous silicon is treated as with regard to claim 10 above. Ogawa, Chu are applied as above.

Fujikura 5,949,271 teaches the shift register circuit or buffer circuit including a bootstrap circuit including thin film transistors. See column 1 lines 6 to column 2 line 18, column 8 lines 6-48, column 13 lines 26-43. The advantages include buffer or shift register circuit capable of operating at high speed.

Accordingly, the claimed invention would have been obvious for the reasons delineated above and additionally, it would have been obvious to have incorporated the bootstrap circuit in the above structure wherein such would have been advantageous to obtain buffer circuit capable of operating at high speed as taught by Fujikura. The use of depletion-mode including channel implant would have been conventional and obvious as evidenced by Ogawa and Chu as delineated above to obtain low power and or enhance accuracy in the buffer circuit and to obtain the desired threshold voltage.

The connection to output terminal in claims 17, 40, 43, and the employment of suitable substrates such as glass or quart in claims 18, 41, 44, would have been obvious for the same reasons delineated above with regard to claims 8, 11, 34, 37, and claims 9, 12, 35, 38, above, respectively.

Application/Control Number: 10/808,344

Art Unit: 2826

Claims 25-32 are 45-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama taken with Ogawa and Chu as applied to claims 7-12 and 33-38 above, and further in view of Yamazaki or Zhang.

Although the prior art above does not recite the metal element promoting crystallization, it would have been obvious to one skilled in the art to have included in the semiconductor a metal element capable of promoting crystallization since such is conventional and advantageous for such purpose as evidenced by Yamazaki, 6,087,758, column 14 lines 37-40 and as evidenced by Zhang the abstract, column 5 lines 57 to column 4, wherein improved operations and reliability can be obtained.

Claims 47-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama taken with Ogawa, Chu, Fujikura as applied to claims 13-18, 39-44 above, and further in view of Yamazaki or Zhang.

Although the prior art above does not recite the metal element promoting crystallization, it would have been obvious to one skilled in the art to have included in the semiconductor a metal element capable of promoting crystallization since such is conventional and advantageous for such purpose as evidenced by Yamazaki, 6,087,758, column 14 lines 37-40 and as evidenced by Zhang 6,077,758, the abstract, column 5 lines 57 to column 4, wherein improved operations and reliability can be obtained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

Application/Control Number: 10/808,344 Page 7

Art Unit: 2826

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach Primary Examiner